Amendments to the claims

Please amend claim 10 as shown in the following listing of claims. This listing of claims will replace all prior versions, and listings, of claims in the application.

1. (original) A semiconductor structure comprising:

a semiconductor core having a side surface;

a layer of insulating material on said side surface; and

electrically isolated electrodes arrayed along said layer of insulating material on said side surface, said electrically isolated electrodes including a conductive material having etch selectivity with respect to said insulating material.

2. (original) The semiconductor structure of claim 1 wherein said electrically isolated electrodes extend substantially in a direction orthogonal to a major surface of said semiconductor core, said major surface being orthogonal to said side surface.

3. (original) The semiconductor structure of claim 1 wherein said conductive material includes silicon-based conductive material.

4. (original) The semiconductor structure of claim 3 wherein said silicon-based conductive material includes polysilicon.

5. (original) The semiconductor structure of claim 1 wherein said semiconductor core includes single-crystal silicon.

6. (original) The semiconductor structure of claim 1 wherein said insulating material of said layer includes oxide of said semiconductor core.

7. (original) The semiconductor structure of claim 1 wherein said electrically isolated electrodes are additionally arrayed over a major surface of said semiconductor core, said major surface being orthogonal to said side surface.

8. (original) The semiconductor structure of claim 7 further comprising interconnects electrically connected to selected ones of said electrically isolated electrodes, said interconnects being positioned over said major surface of said semiconductor core.

9. (original) The semiconductor structure of claim 7 wherein said electrically isolated electrodes are additionally arrayed along a second side surface of said semiconductor core.

10. (currently amended) A semiconductor structure comprising:

a semiconductor core having a major surface and a side surface, said major surface being orthogonal to said side surface;

a continuous layer of insulating material on said side surface; and

electrically isolated electrodes arrayed along said continuous layer of insulating material on said side surface such that said electrically isolated electrodes extend substantially in a direction orthogonal to said major surface, said electrically isolated electrodes including conductive material having etch selectivity with respect to said insulating material.

11. (original) The semiconductor structure of claim 10 wherein said conductive material includes silicon-based conductive material.

12. (original) The semiconductor structure of claim 11 wherein silicon-based conductive material includes doped polysilicon.

13. (original) The semiconductor structure of claim 10 wherein said semiconductor core includes single-crystal silicon.

14. (original) The semiconductor structure of claim 10 wherein said electrically isolated electrodes additionally extend over said major surface of said semiconductor core.

15. (original) The semiconductor structure of claim 14 further comprising interconnects electrically connected to selected ones of said electrically isolated electrodes, said interconnects being positioned over said major surface of said semiconductor core.

16. (withdrawn) A method for fabricating a semiconductor structure, the method comprising:

providing a semiconductor core with a side surface;

forming a layer of insulating material on said side surface of said semiconductor core;

forming a layer of conductive material adjacent to said layer of insulating material on said side surface, said conductive material having etch selectively with respect to said insulating material; and

selectively etching said layer of conductive material using a stop-on-oxide deep reactive ion etching to define electrically isolated electrodes arrayed along said layer of insulating material on said side surface.

17. (withdrawn) The method of claim 16 wherein said selectively etching includes selectively etching said layer of conductive material using said stop-on-oxide deep reactive ion etching such that said electrical isolated electrodes extend substantially in a direction orthogonal to a major surface of said semiconductor core, said major surface being orthogonal to said side surface.

18. (withdrawn) The method of claim 16 wherein said forming of said layer insulating material includes forming a layer of oxide on said side surface of said semiconductor core.

19. (withdrawn) The method of claim 16 wherein said forming of said layer of conductive material includes forming a layer of silicon-based conductive material adjacent to said layer of insulating material.

20. (withdrawn) The method of claim 19 wherein said forming of said layer of silicon-based conductive material includes forming a layer of polysilicon adjacent to said layer of insulating material.

21. (withdrawn) The method of claim 16 wherein said providing of said semiconductor core includes providing a single-crystal silicon core with said side surface.

22. (withdrawn) The method of claim 16 wherein said forming of said layer of conductive material includes forming said layer of conductive material over a major surface of said semiconductor core, said major surface being orthogonal to said side surface, and wherein said selectively etching of said layer of conductive material includes selectively etching said layer of conductive material over said major surface of said semiconductor core using said stop-on-oxide deep reactive ion etching such that said electrically isolated electrodes extend over said major surface of said semiconductor core.

23. (withdrawn) The method of claim 22 further comprising forming interconnects over said major surface of said semiconductor core, said interconnects being electrically connected to selected ones of said electrically isolated electrodes.